Impact of CMOS Technologies scaling in Leakage Reduction Techniques

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Outline

- Introduction
- Background
- Approach
- Results
- Contribution
- Future Work

Introduction

- Motivation
  - Power consumption is the major concern in CMOS circuits.
  - Leakage is one of the big part of power consumption.
  - Leakage current is getting a really serious problem as the technology size shrinks.
- Goals
  - Explore what conventional techniques for leakage reduction is used and see their effectiveness with new and future technologies.
  - Construct a curve or graph which can be used to extrapolate pareto curves.

Sleep Technique

- Pros
  - Low impact on dynamic operations
  - Pretty effective in sleep mode
- Cons
  - Additional area
  - Different signal
  - Wake up energy and delay
  - Only reduce leakage during sleep
- Knobs
  - Footer vs. Header (NMOS vs. PMOS)
  - Width
  - Sharing vs. Non-sharing

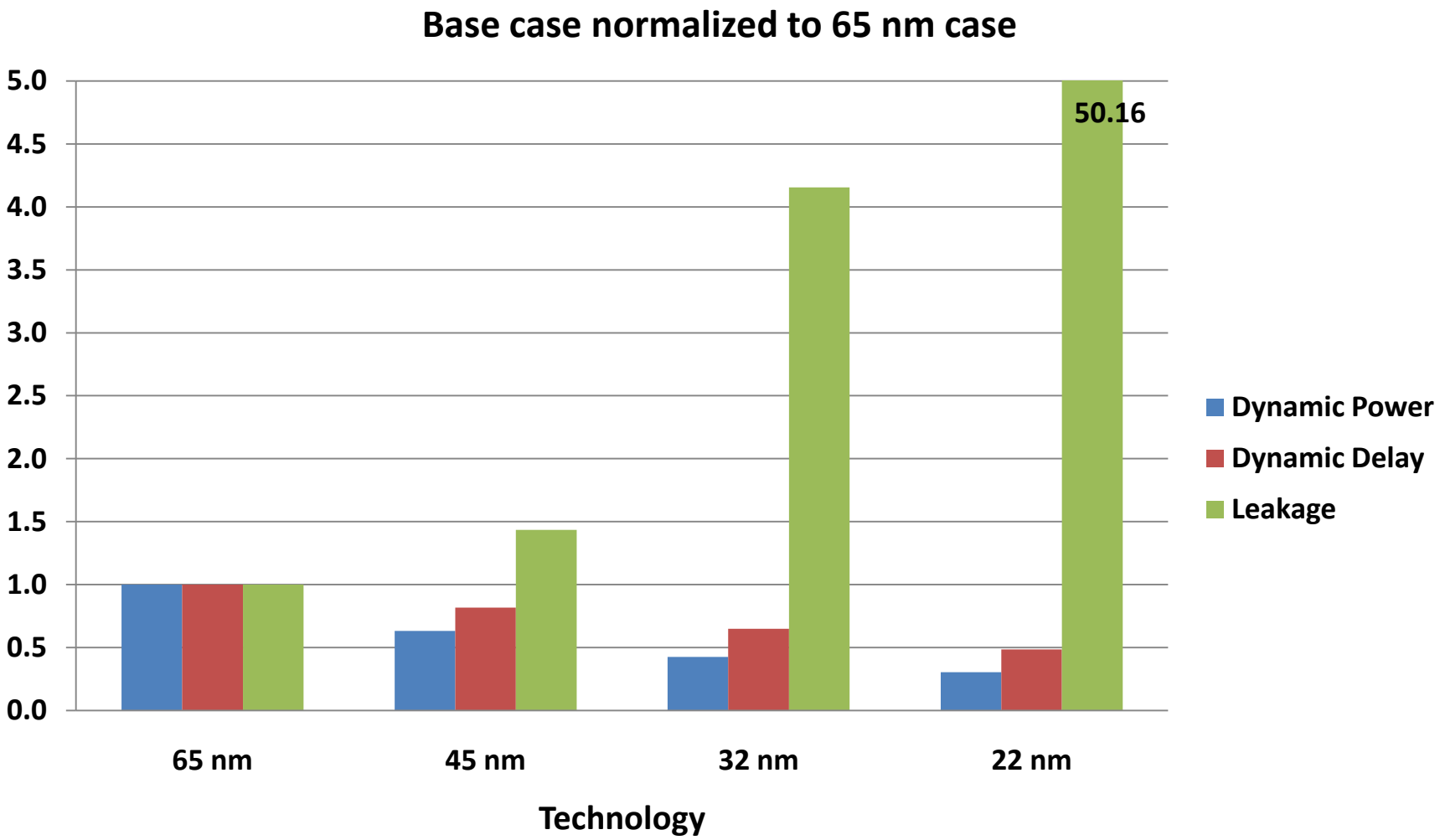
Stack Technique

- Pros
  - No need to go to sleep mode
- Cons
  - Huge impact on dynamic operations
  - Big area cost
- Knobs
  - Width
  - Placement: Headers vs footers, some inputs.

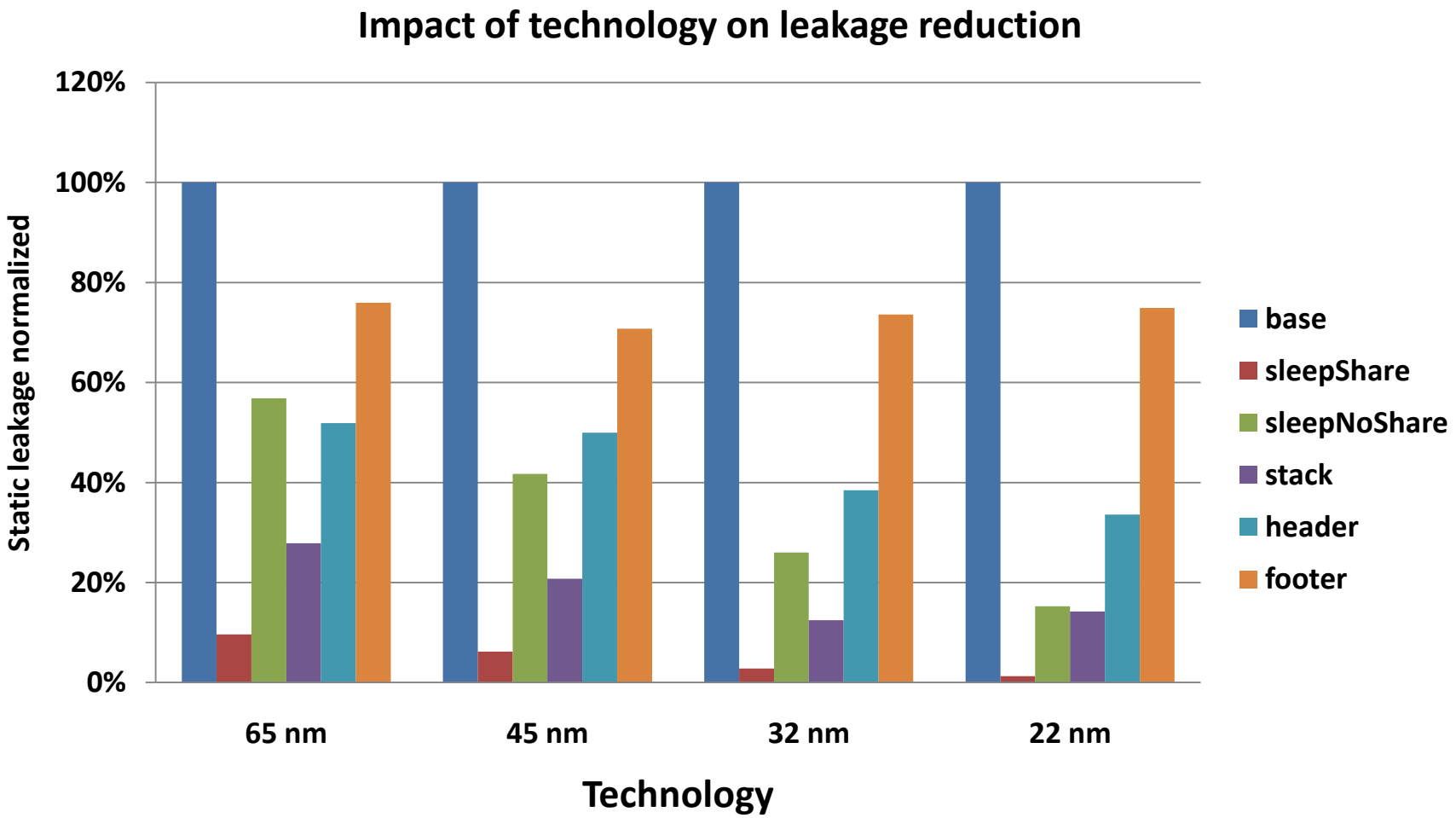
Approach

- Simulated circuit
  - Simulate glitching
  - Large enough to be between 2 registers stages
  - Not fully accurate, but good enough
- Dynamic delay
  - Dynamic Delay, 50% of input to 50% of output, averaged between the two transitions 0->1 and 1->0
- Dynamic energy
  - Dynamic Energy, averaged between 0->1, 1->0
  - Leakage Energy, averaged between static 0, 1
- Variation
  - 50 Monte Carlo iterations

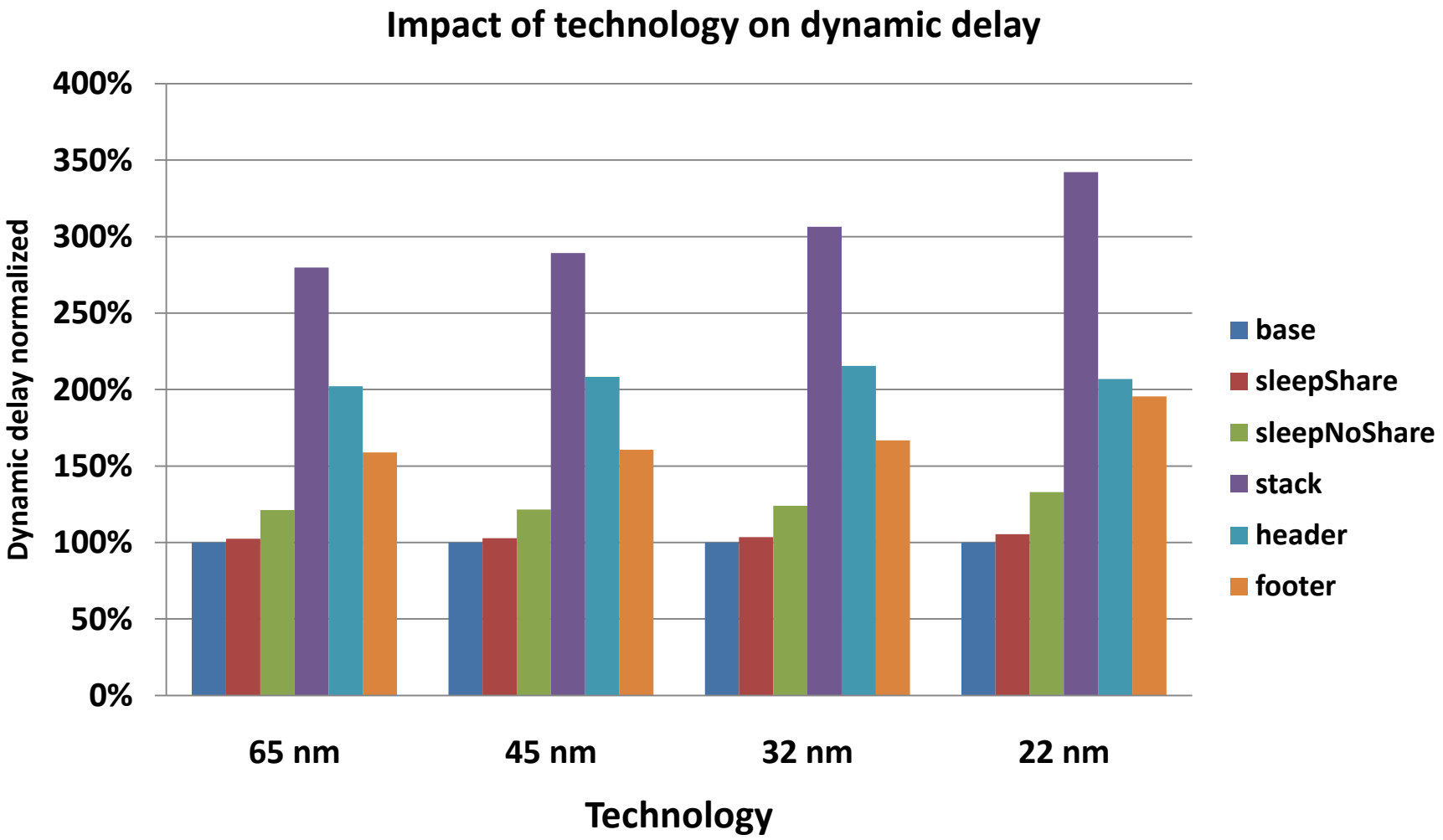
Leakage predictions



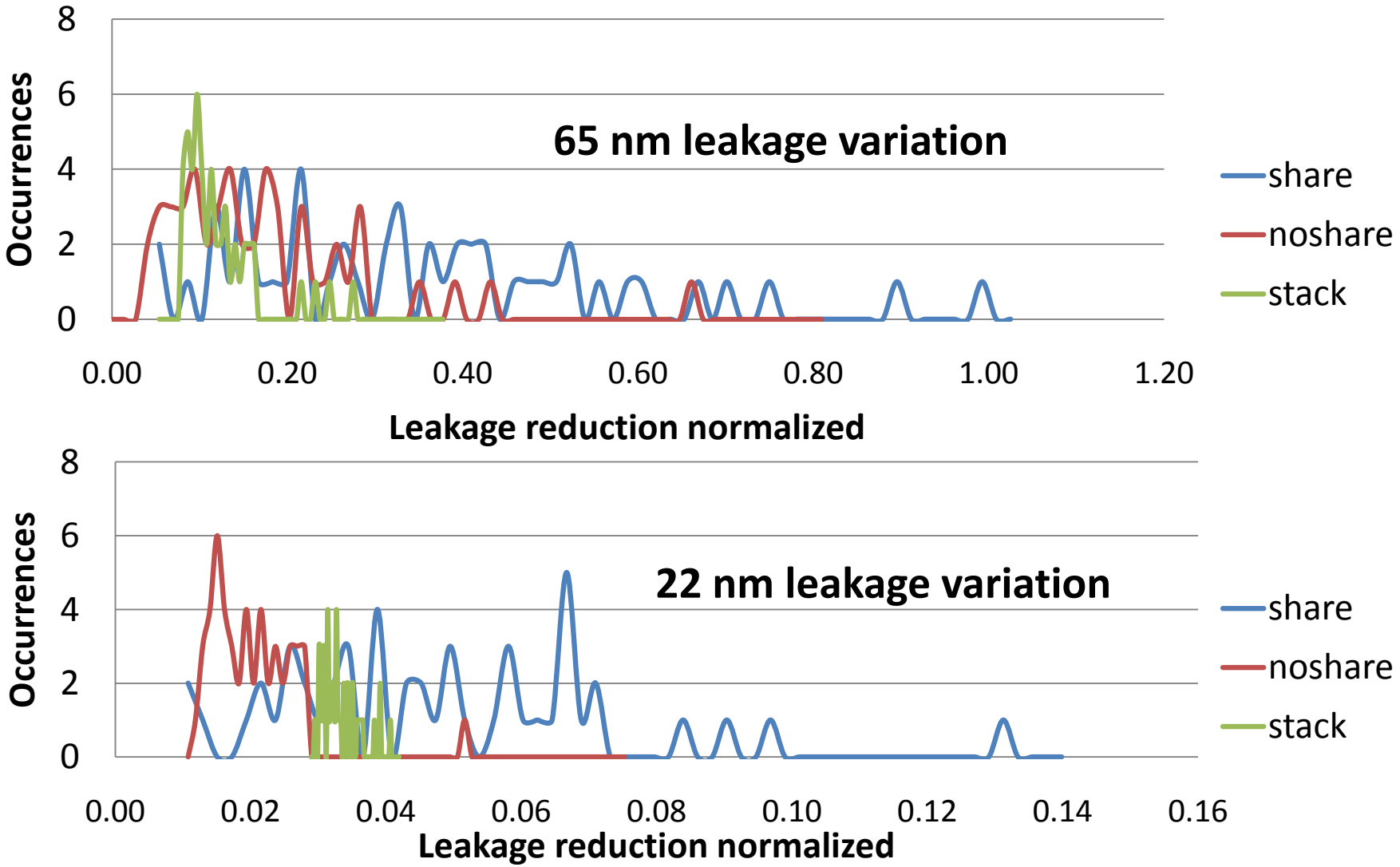
Leakage reduction techniques vs. technology



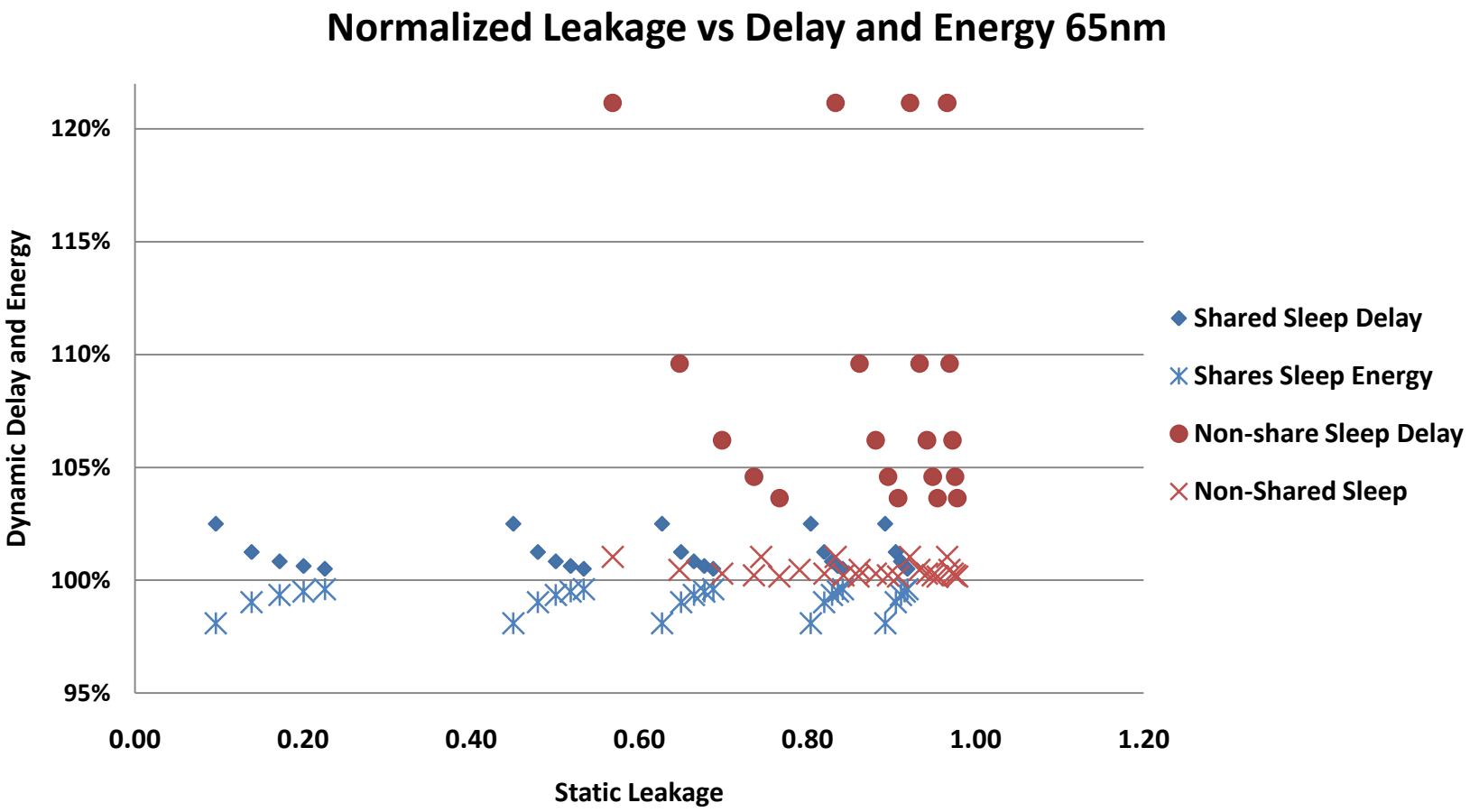
Delay vs. Technology



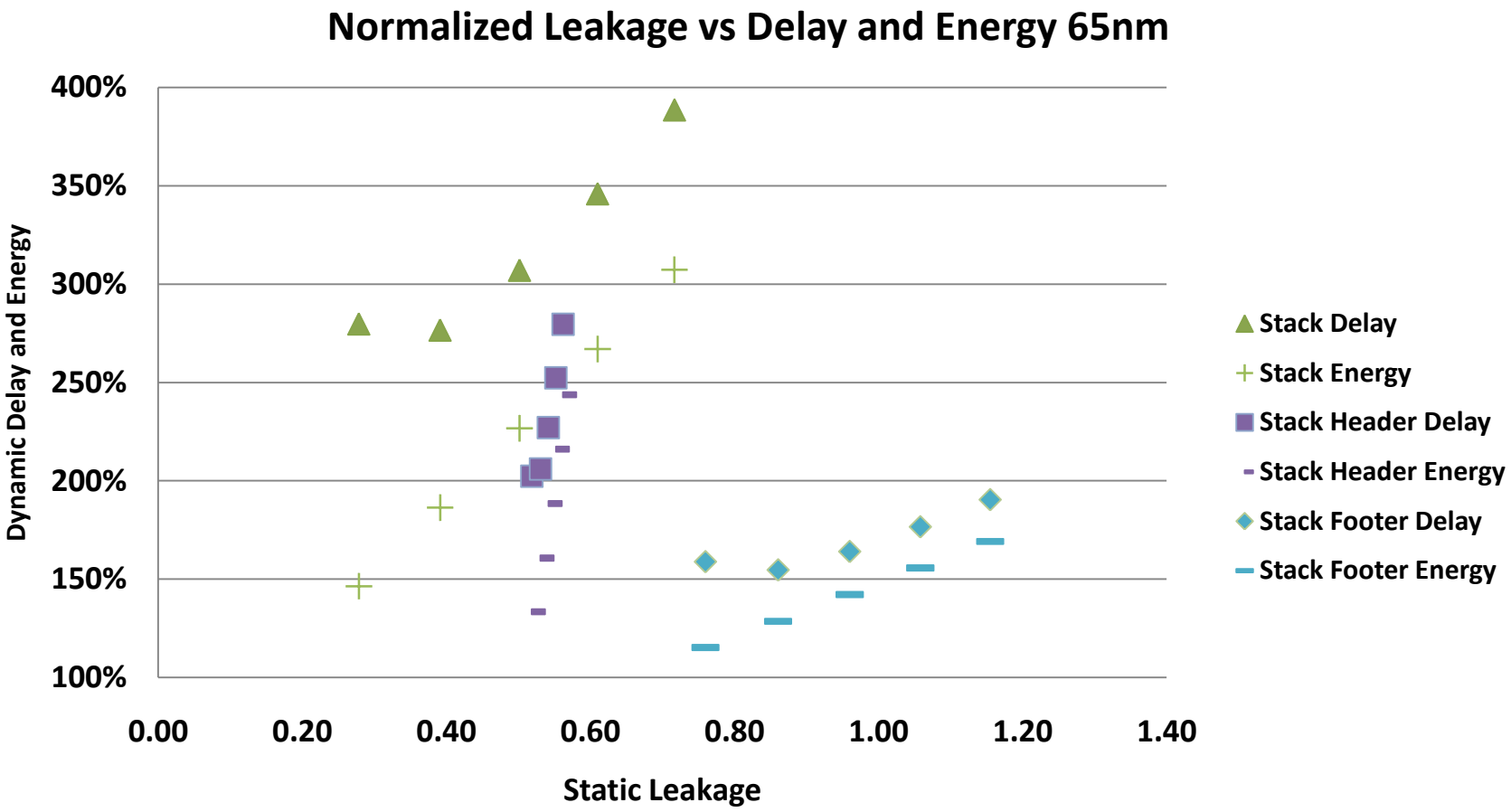
Leakage reduction variation



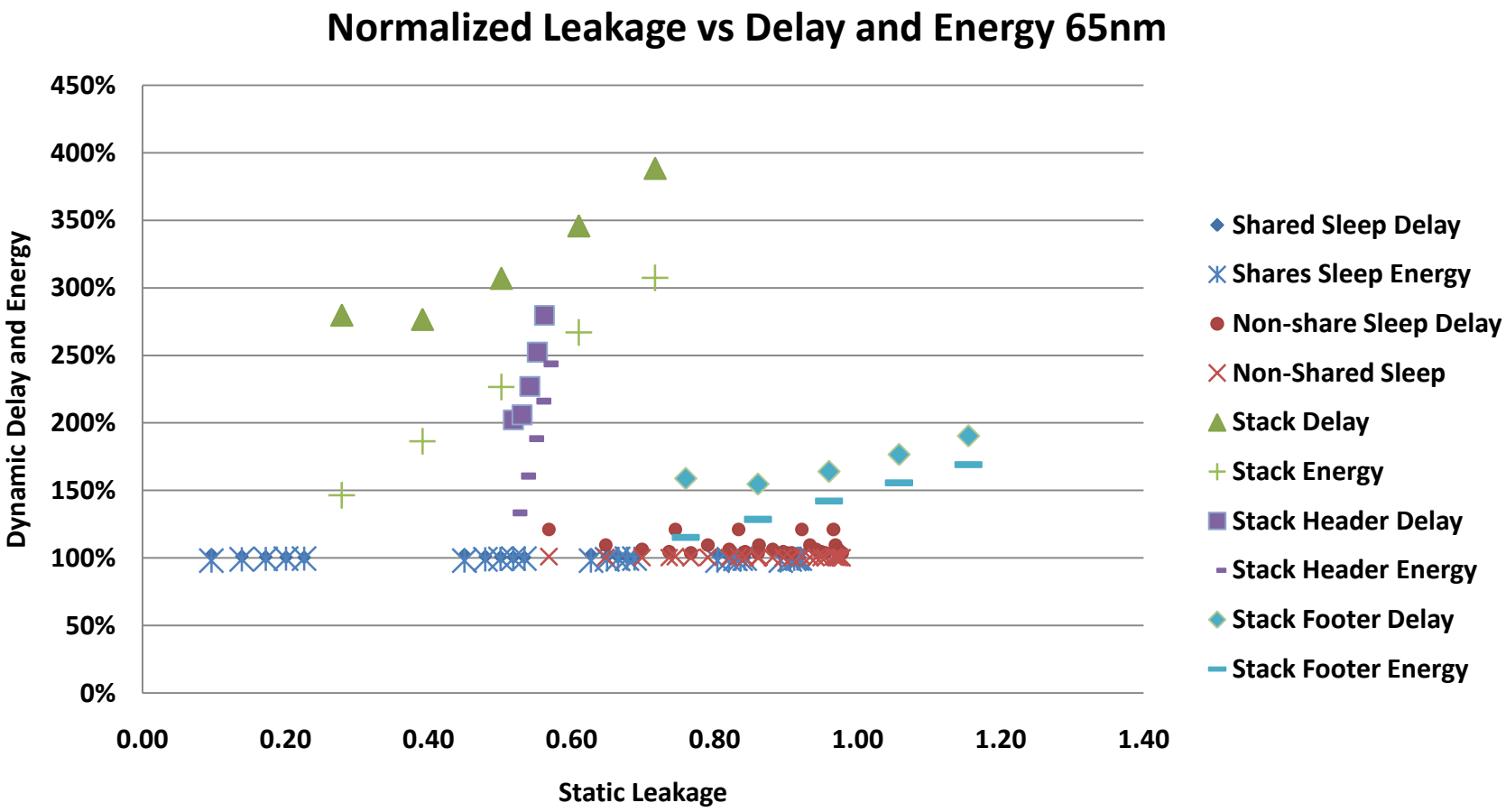
Sleep Technique



Stack Technique



Pareto Curve



Comparison

Metric	Stack	Sleep
Added delay	High	Low
Added energy	High	Low
Leakage in active mode	Medium	None
Leakage in sleep	Medium	High
Complexity	Simple	Complex
Area	Big area	Medium area

Contribution

- Explored the performance of some leakage techniques under future technologies
- Suggested several knobs to be tweaked to achieve the desired performance
- Constructed a generic pareto curve which can be used to extract the parameters needed to achieve a specific performance and cost

Future Work

- Analysis of the other techniques using more general circuit, such as full adder and SRAM.
- Analysis of different set of knobs like placement location and voltage threshold.
- Explore if changing VDD might affect the performance of the techniques
- Evaluation of new scaling technologies (16nm) or using other Predictive Technology Model.

The End

Questions?